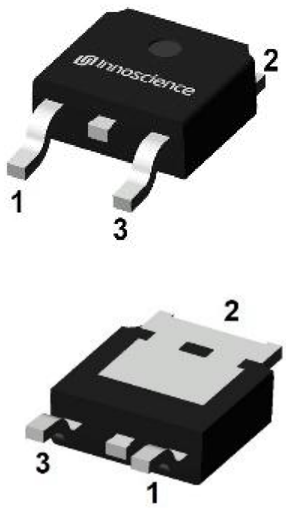
INN900TK350B

1. General description

900V GaN-on-Silicon Enhancement-mode Power Transistor in TO-252 package.

2. Features

- Enhancement mode transistor-Normally off power switch
- Ultra high switching frequency
- No reverse-recovery charge
- Low gate charge, low output charge
- Qualified for industrial applications according to JEDEC Standards
- ESD safeguard
- RoHS, Pb-free, REACH-compliant



3. Applications

- AHB/LLC/ACF Converter for Fast battery charger
- QR Flyback Converter for Fast battery charger
- Optimized to withstand high voltage transients in unstable mains network

4. Key performance parameters

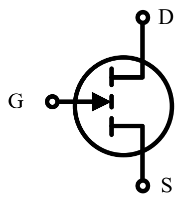


Table 1 Key performance parameters at T_j = 25 °C

Parameter	Value	Unit
$V_{DS,max}$	900	V
$R_{DS(on),max}$ @ V_{GS} = 6 V	350	mΩ
$Q_{G,typ}$ @ V_{DS} = 400 V	1.5	nC
$I_{D,pulse}$	10	A
Q_{OSS} @ V_{DS} = 400 V	16.5	nC
Q_{rr} @ V_{DS} = 400 V	0	nC

5. Pin information

Table 2 Pin information

Gate	Source	Drain
1	2	3

Table 3 Ordering information

Type/Ordering Code	Package	Product Code
INN900TK350B	TO-252	90TK350B

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6. Maximum ratings

at T_j = 25 °C unless otherwise specified.

Continuous application of maximum ratings can deteriorate transistor lifetime. For further information, contact Innoscience sales office.

Table 4 Maximum ratings

Parameter	Symbol	Values	Unit	Note/Test Condition
Drain source voltage	$V_{DS,max}$	900	V	V_{GS} = 0 V, T_j = -55 °C to 150 °C
Continuous current, drain source	I_D	6	A	T_c = 25 °C
Pulsed current, drain source [1]	$I_{D,pulse}$	10	A	T_c = 25 °C; V_{GS} = 6 V; t_{PULSE} = 10 µs
Pulsed current, drain source [1]	$I_{D,pulse}$	6	A	T_c = 125 °C; V_{GS} = 6 V; t_{PULSE} = 10 µs
Gate source voltage, continuous [2]	V_{GS}	-1.4 to +7	V	T_j = -55 °C to 150 °C
Gate source voltage, pulsed	$V_{GS,pulse}$	-20 to +10	V	T_j = -55 °C to 150 °C; t_{PULSE} = 50 ns, f = 100 kHz; open drain
Power dissipation	P_{tot}	60	W	T_c = 25 °C
Operating temperature	T_j	-55 to +150	˚C	
Storage temperature	T_{stg}	-55 to +150	˚C	

1 Limit was extracted from characterization test, not measured during production

2 The minimum V_{GS} is clamped by ESD protection circuit, as shown in Figure 10

7. Thermal characteristics

Table 5 Thermal characteristics

Parameter	**Symbol**	**Values**	**Unit**	**Note/Test Condition**
Thermal resistance, junction-ambient	R_{thJA}	45	°C/W	
Thermal resistance, junction-case	R_{thJC}	2.05	°C/W	
Maximum reflow soldering temperature	T_{sold}	260	°C	MSL3

1.R_{thJA} is determined with the device mounted on one square inch of copper pad, single layer 2oz copper on FR4 board.

8. Electric characteristics

at T_j = 25 °C, unless specified otherwise

Table 6 Static characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(th)}$	1.2	1.7	2.5	V	I_D = 7.4 mA; V_{DS} = V_{GS}; T_j = 25 °C
		-	1.6	-		I_D = 7.4 mA; V_{DS} = V_{GS}; T_j = 150 °C
Drain-source leakage current	I_{DSS}	-	0.6	15	μA	V_{DS} = 720 V; V_{GS} = 0 V; T_j = 25 °C
		-	5	-		V_{DS} = 720 V; V_{GS} = 0 V; T_j = 150 °C
Gate-source leakage current	I_{GSS}	-	40	-	μA	V_{GS} = 6 V; V_{DS} = 0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	265	350	mΩ	V_{GS} = 6 V; I_D = 2.2 A; T_j = 25 °C
		-	583	-	mΩ	V_{GS} = 6 V; I_D = 2.2 A; T_j = 150 °C
Gate resistance	R_G	-	8	-	Ω	f = 5 MHz; open drain

Table 7 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	54	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100 kHz
Output capacitance	C_{oss}	-	21	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100 kHz
Reverse transfer Capacitance	C_{rss}	-	0.2	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100 kHz
Effective output capacitance, energy related [1]	$C_{o(er)}$	-	29	-	pF	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Effective output capacitance, time related [2]	$C_{o(tr)}$	-	40	-	pF	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Output charge	Q_{OSS}	-	16.5	-	nC	V_{GS} = 0 V; V_{DS} = 0 to 400 V

1. $C_{O(er)}$ is the fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V
2. $C_{O(tr)}$ is the fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V

Table 8 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate charge	Q_G	-	1.5	-	nC	V_{GS} = 0 to 6 V; V_{DS} = 400 V; I_D= 2.2 A
Gate-source charge	Q_{GS}	-	0.12	-	nC	
Gate-drain charge	Q_{GD}	-	0.5	-	nC	
Gate Plateau Voltage	V_{Plat}	-	2.2	-	V	V_{DS} = 400 V; I_D= 2.2 A

Table 9 Reverse conduction characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Source-Drain reverse voltage	V_{SD}	-	3.5	-	V	V_{GS} = 0 V; I_S = 2.2 A
Pulsed current, reverse	$I_{S,pulse}$	-	-	14	A	V_{GS} = 6 V; t_{PULSE} = 10 μs
Reverse recovery charge	Q_{rr}	-	0	-	nC	I_S = 2.2 A; V_{DS} = 400 V
Reverse recovery time	t_{rr}	-	0	-	ns	
Peak reverse recovery current	I_{rrm}	-	0	-	A	

9. Electric characteristics diagrams

at T_j = 25 °C, unless specified otherwise

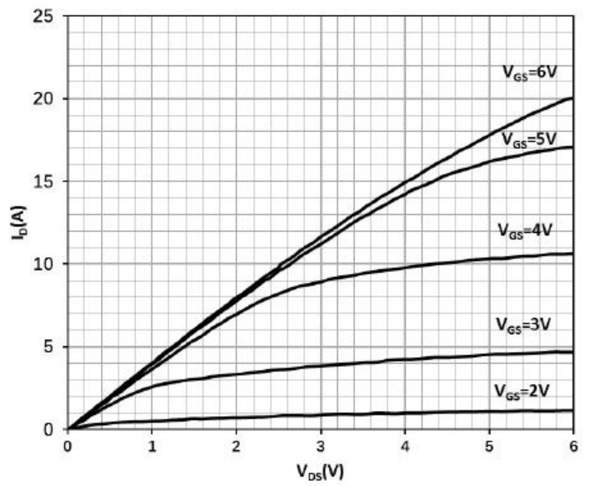
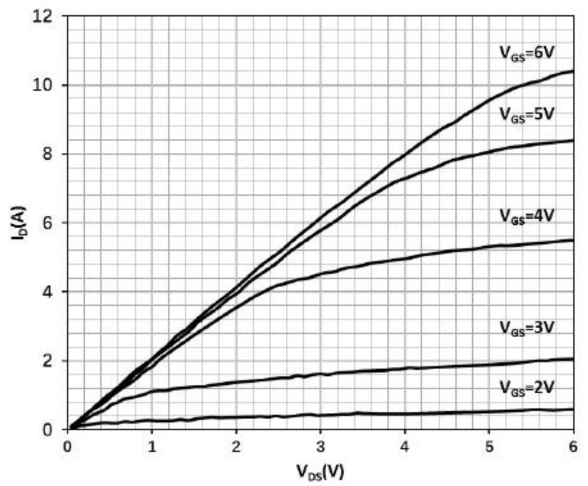
Figure 1 Typ. output characteristics	Figure 2 Typ. output characteristics
	
$I_D = f(V_{DS},V_{GS})$; T_j = 25 °C	$I_D = f(V_{DS},V_{GS})$; T_j = 125 °C

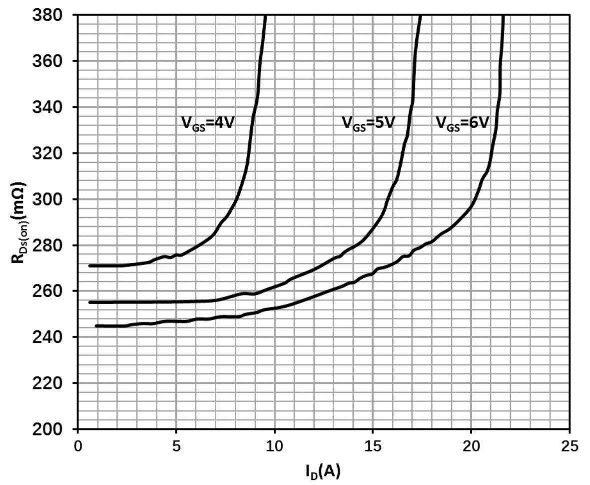
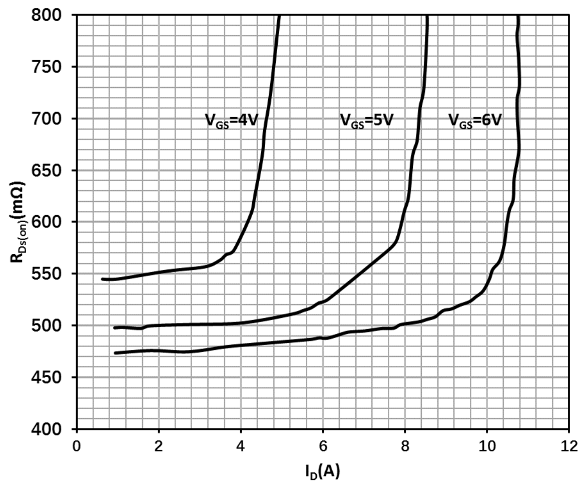
Figure 3 Typ. Drain-source on-state resistance	Figure 4 Typ. Drain-source on-state resistance
	
$R_{DS(on)} = f(I_{DS},V_{GS})$; T_j = 25 °C	$R_{DS(on)} = f(I_{DS},V_{GS})$; T_j = 125 °C

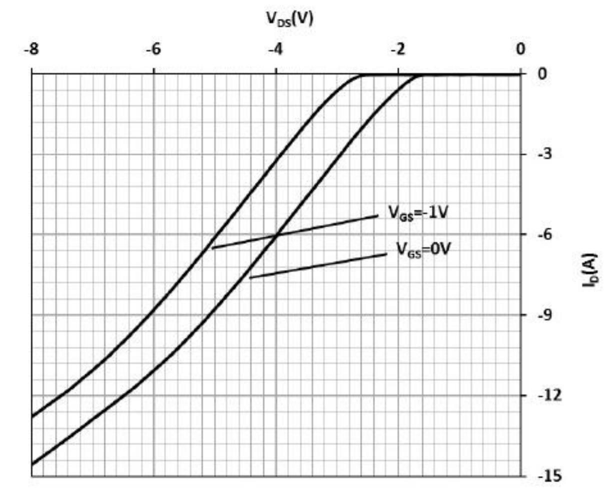
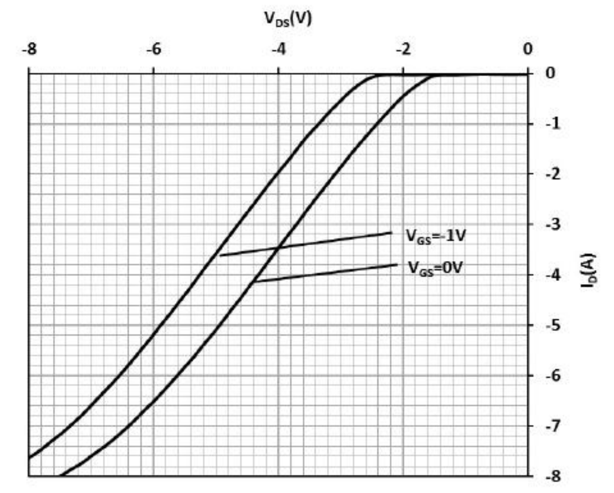
Figure 5 Typ. channel reverse characteristics	Figure 6 Typ. channel reverse characteristics
	
$I_D = f(V_{DS},V_{GS})$; T_j= 25 °C	$I_D = f(V_{DS},V_{GS})$; T_j = 125 °C

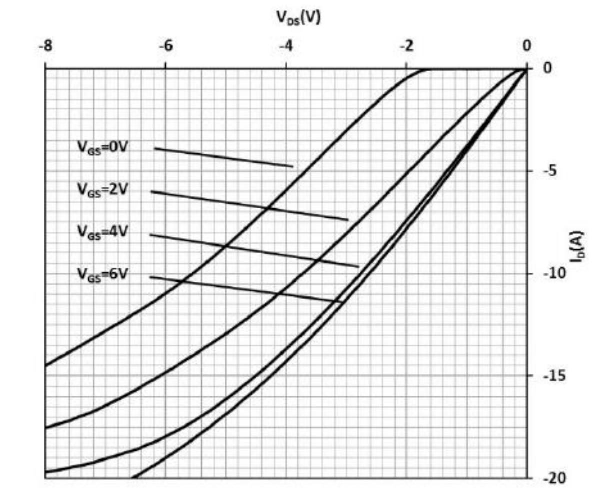
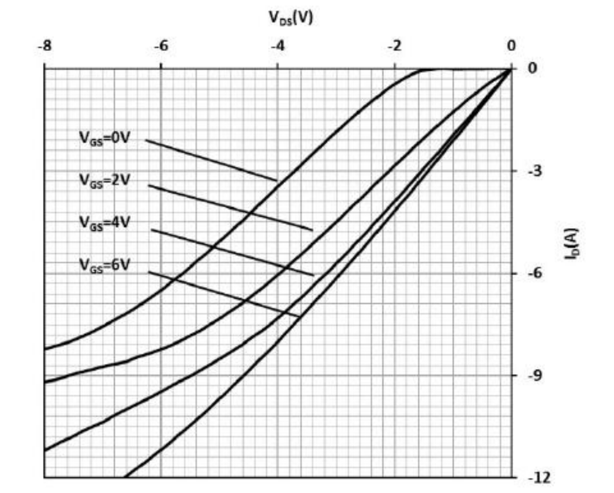
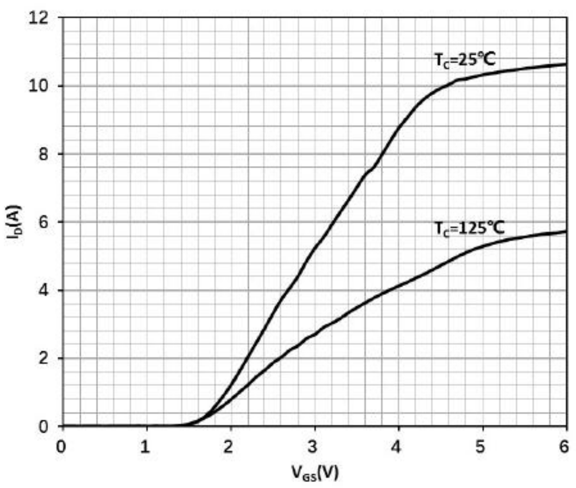
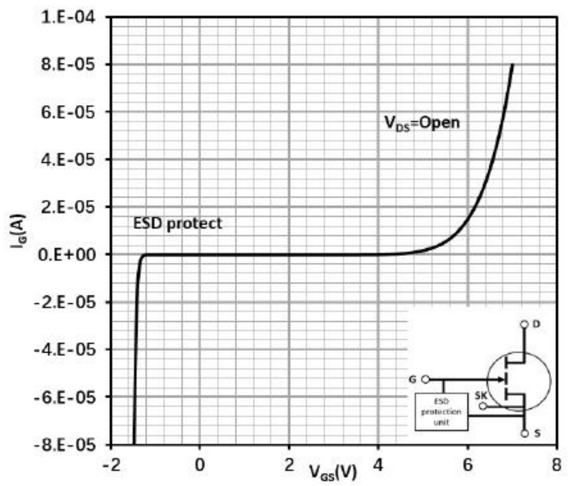
Figure 7 Typ. channel reverse characteristics	Figure 8 Typ. channel reverse characteristics
	
$I_D = f(V_{DS},V_{GS})$; T_j = 25 °C	$I_D = f(V_{DS},V_{GS})$; T_j = 125 °C

Figure 9   Typ. transfer characteristics



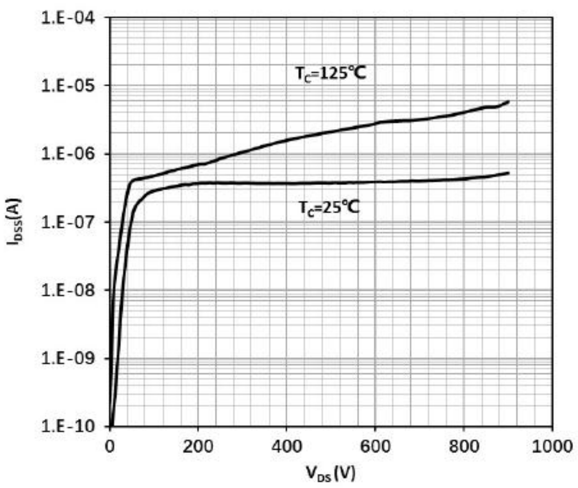
$I_D = f(V_{GS})$; V_{DS}= 3 V

Figure 10   Typ. Gate-to-Source leakage



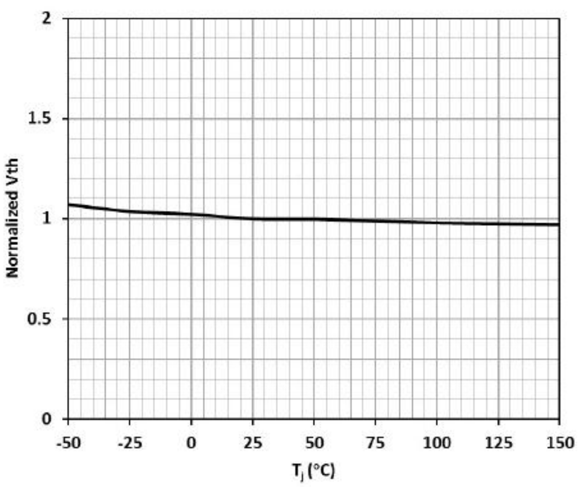
$I_G = f(V_{GS})$; I_G reverse turn on by ESD unit

Figure 11   Drain-source leakage characteristics



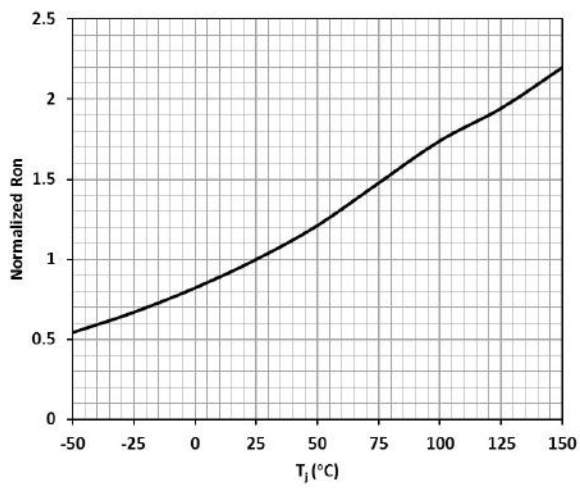
$I_{DSS} = f(V_{DS})$; V_{GS} = 0 V

Figure 12 Gate threshold voltage



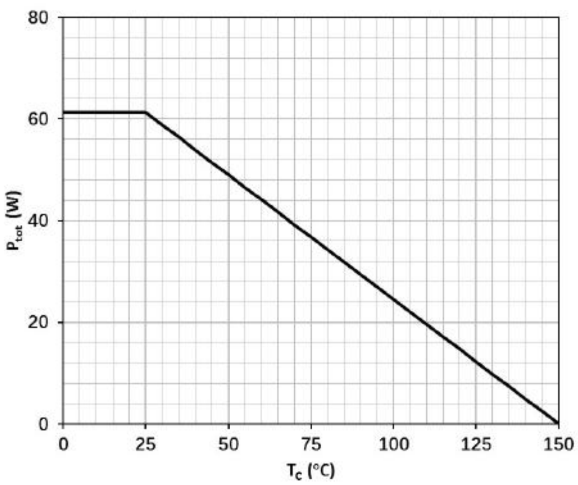
$V_{TH} = f(T_j)$; $V_{GS} = V_{DS}$; I_D = 7.4 mA

Figure 13 Drain-source on-state resistance



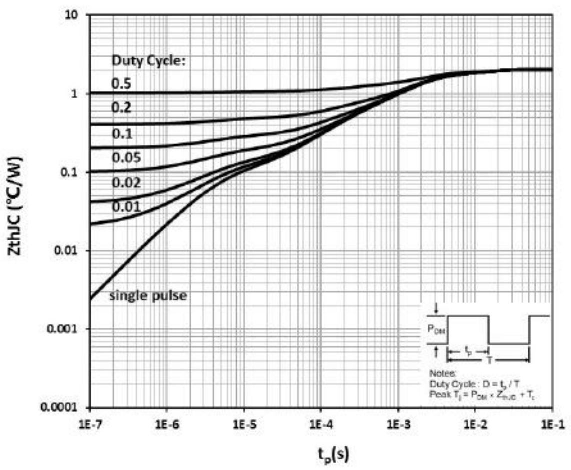
$R_{DS(on)} = f(T_j)$; I_D = 2.2 A; V_{GS}=6V

Figure 14 Power dissipation



$P_{tot} = f(T_C)$

Figure 15 Max.transient thermal impedance



$Z_{thJC} = f(t_P, D)$

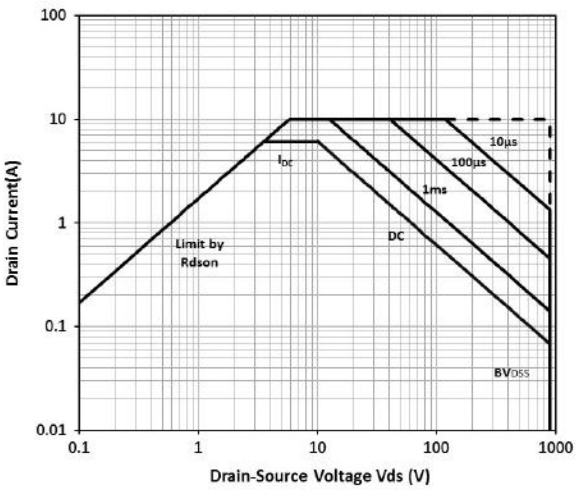
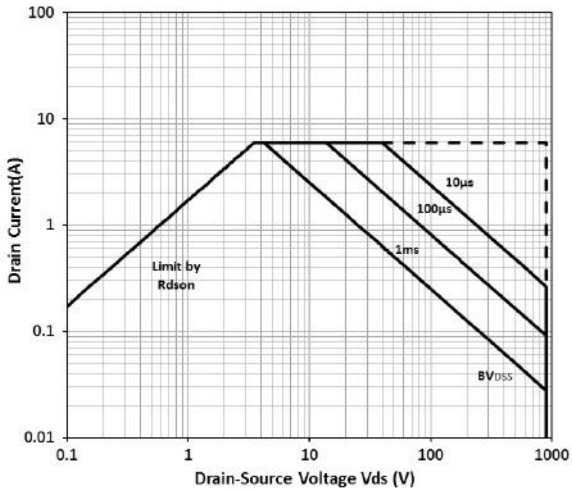
Figure 16 Safe operating area	Figure 17 Safe operating area
	
$I_D = f(V_{DS})$; T_C = 25 °C	$I_D = f(V_{DS})$; T_C = 125 °C

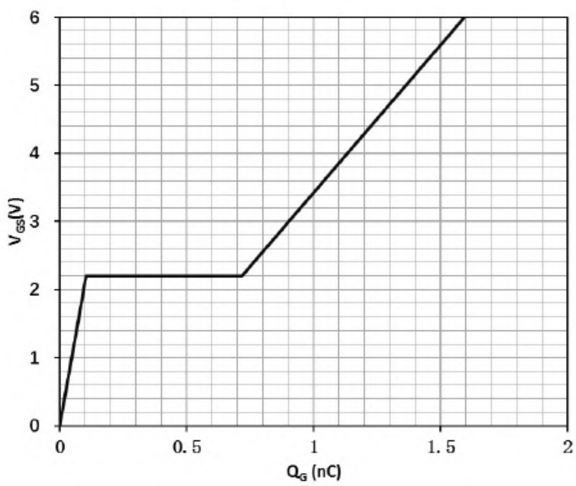
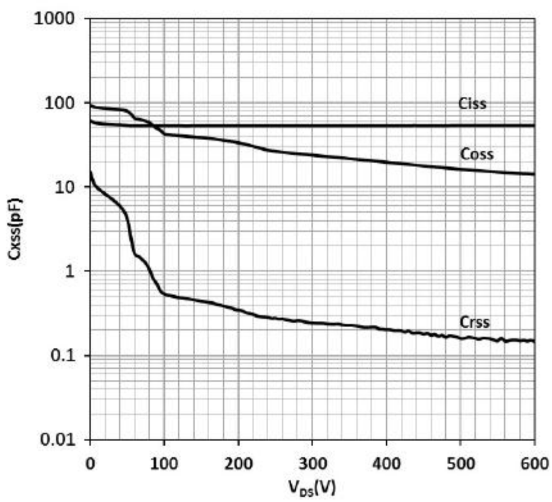
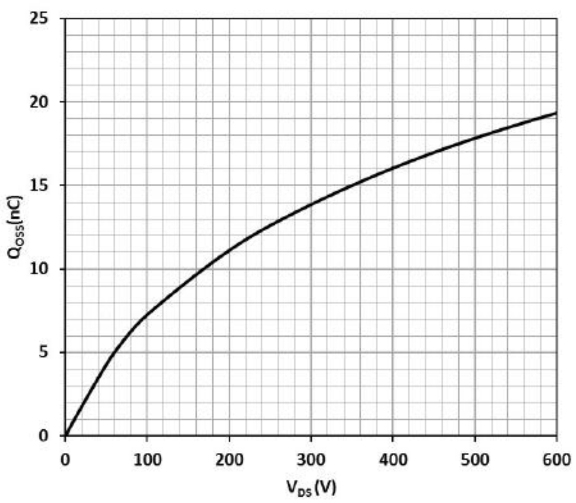
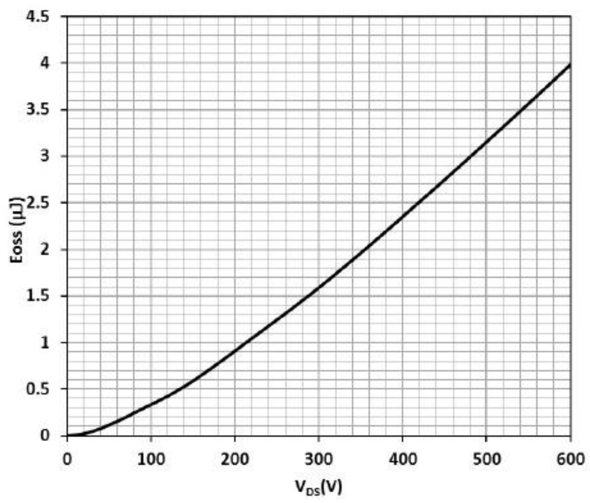
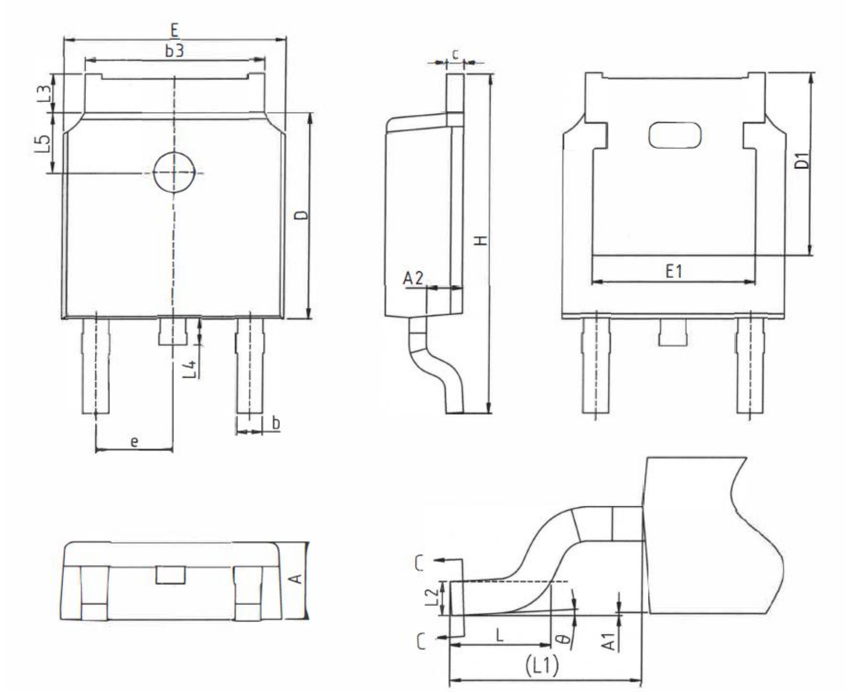
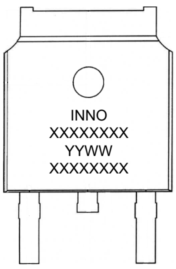
Figure 18 Typ. gate charge	Figure 19 Typ. capacitances
	
$V_{GS} = f(Q_G)$; V_{DCLINK} = 400 V; I_D = 2.2 A	$C_{XSS} = f(V_{DS})$; Freq. = 100 kHz

Figure 20 Typ. output charge	Figure 21 Typ. C_{OSS} stored Energy
	
$Q_{OSS} = f(V_{DS})$; Freq. = 100 kHz	$E_{OSS} = f(V_{DS})$; Freq. = 100 kHz

10. Package outlines



SYMBOL	MM			SYMBOL	MM		
	MIN	NOM	MAX		MIN	NOM	MAX
A	2.20	2.30	2.40	e	2.286BSC		
A1	0.00	-	0.13	H	9.40	10.10	10.50
A2	0.92	1.07	1.17	L	1.38	1.50	1.75
b	0.63	0.78	0.90	L1	2.90REF		
b3	5.10	5.33	5.46	L2	0.51BSC		
c	0.43	0.53	0.61	L3	0.88	-	1.28
D	5.98	6.10	6.22	L4	0.50	-	1.00
D1	5.30REF			L5	1.65	1.80	1.95
E	6.40	6.60	6.73	θ	0°	-	8°
E1	4.83REF						



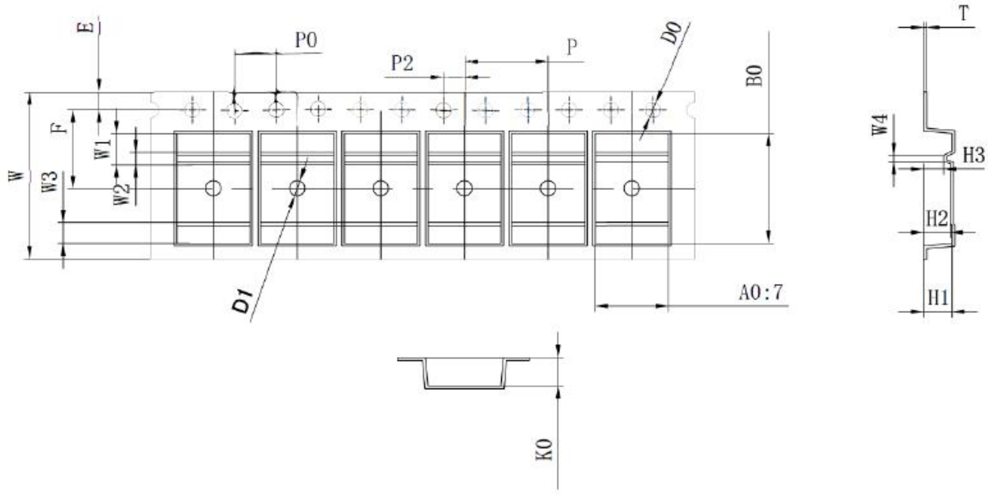
ROW	Description	Example
Row1	Company name	INNO
Row2	Product code	XXXXXXXX
Row3	Date code	YYWW
Row4	ASSY lot No.	XXXXXXXX

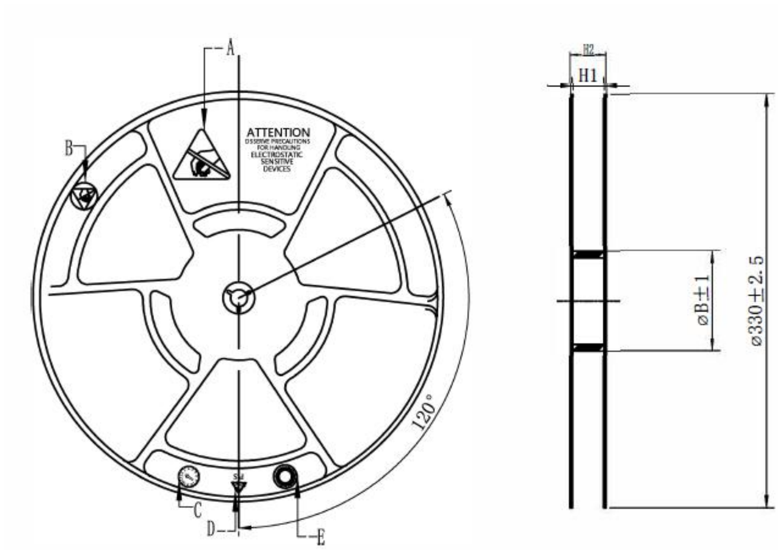
Notes:
(1) All dimension are in millimeters.
(2) Drawing is not to scale.
(3) Dimensions do not include mold protrusion.
(4) Package outline exclusive of metal burr dimensions.

11. Reel information

DATA	W	T	P	A_0	B_0	K_0	K_1	E	F	P_0	P_2	D_0	D_1	W_1	W_2	W_3	H_1	H_2	H_3	W_4
	16.0 +0.40 −0.20	0.30 +0.05 −0.05	8.00 +0.15 −0.15	7.00 +0.20 −0.20	10.50 +0.15 −0.15	2.70 +0.15 −0.15	0.00 +0.10 −0.10	1.75 +0.15 −0.15	7.50 +0.15 −0.15	4.00 +0.13 −0.13	2.00 +0.15 −0.15	1.55 +0.13 −0.13	1.50 +0.25 −0.25	3.0 +0.15 −0.15	1.2 +0.13 −0.13	2.0 +0.15 −0.15	2.7 +0.15 −0.15	2.5 +0.15 −0.15	1.7 +0.15 −0.15	0.6 +0.15 −0.15

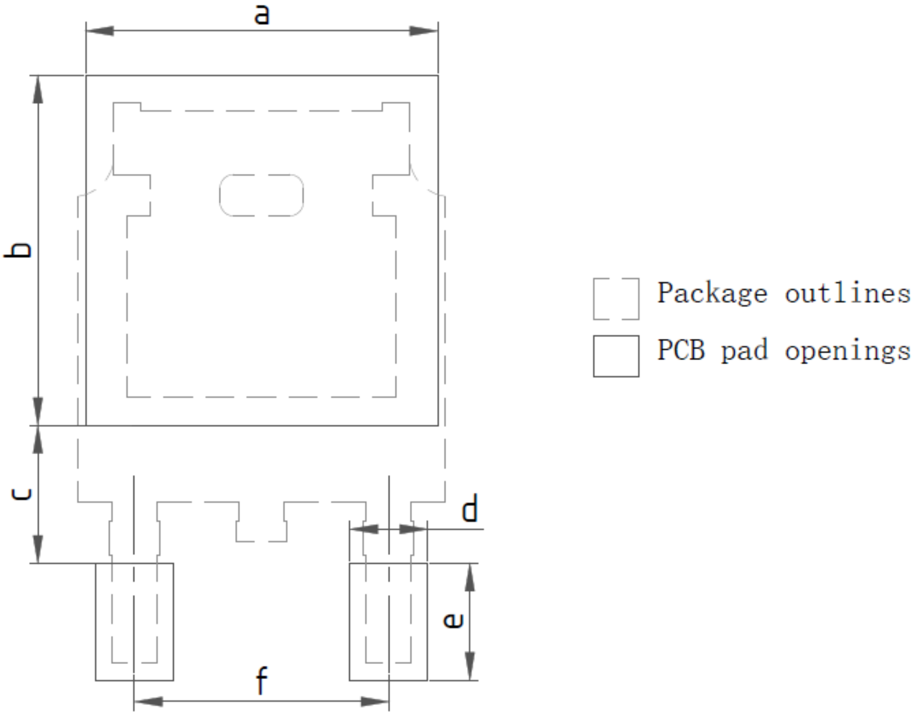
Unit:mm





Unit:	mm
Tape Width	16
H1	16.4±0.1
H2MAX	22.4

12. Recommended PCB footprint



SYMBOL	DIMENSION	SYMBOL	DIMENSION
a	6.33	d	1.40
b	6.30	e	2.10
c	2.48	f	4.57

Notes:
(1)All dimension are in millimeters.
(2)Drawing is not to scale.

13. Revision history

Major changes since the last revision

Revision	Date	Description of changes
1.0	2024-06-04	1.0 version release
1.1	2024-07-31	Update Igss@25℃ typ. value

Important Notice